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# Impact of field-induced quantum confinement on the onset of tunneling field-effect transistors: Experimental verification

Quentin Smets,[1,2,a)] Anne S. Verhulst,[1] Koen Martens,[1] Han Chung Lin,[1] Salim El Kazzi,[1] Devin Verreck,[1,2] Eddy Simoen,[1] Nadine Collaert,[1] Aaron Thean,[1] Jean-Pierre Raskin,[3] and Marc M. Heyns[1,2]

[1]*Imec, Kapeldreef 75, 3001 Heverlee, Belgium*
[2]*KULeuven, 3000 Leuven, Belgium*
[3]*ICTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium*

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The Tunneling Field-Effect Transistor (TFET) is a promising device for future low-power logic. Its performance is often predicted using semiclassical simulations, but there is usually a large discrepancy with experimental results. An important reason is that Field-Induced Quantum Confinement (FIQC) is neglected. Quantum mechanical simulations show FIQC delays the onset of Band-To-Band Tunneling (BTBT) with hundreds of millivolts in the promising line-TFET configuration. In this letter, we provide experimental verification of this delayed onset. We accomplish this by developing a method where line-TFET are modeled using highly doped MOS capacitors (MOS-CAP). Using capacitance-voltage measurements, we demonstrate AC inversion by BTBT, which was so far unobserved in MOS-CAP. Good agreement is shown between the experimentally obtained BTBT onset and quantum mechanical predictions, proving the need to include FIQC in all TFET simulations. Finally, we show that highly doped MOS-CAP is promising for characterization of traps deep into the conduction band. © *2014 AIP Publishing LLC*.
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In the pursuit of CMOS transistor scaling and lowering power consumption, the tunneling field-effect transistor (TFET) has emerged as a promising alternative to MOSFET.[1] It can operate at lower supply voltage because of its steep subthreshold swing (SS) <60 mV/dec, made possible by the energy filtering of band-to-band tunneling (BTBT). Currently, simulations help in the selection of suitable materials and configuration, but there is still a large discrepancy between these simulations and corresponding experimental results.[2] In an effort to reduce this gap, BTBT calibration efforts are ongoing,[3,4] but these are challenging when BTBT occurs towards regions where charge carriers are confined. This is the case in all TFET configurations, where the tunneling direction is at least partially oriented towards the gate stack, such that a triangular-like potential well is formed in the semiconductor at the oxide, causing field-induced quantum confinement (FIQC).[5] In particular, the tunneling direction is fully perpendicular to the gate in the promising line-TFET configuration[6–8] (Fig. 1(a)). The large and uniform electric field in the direction of tunneling allows steeper SS than conventional TFET, but also leads to increased FIQC. It has been predicted, without experimental verification, that FIQC mainly causes a delayed onset of BTBT.[5] In this letter, we experimentally demonstrate this delay of BTBT. To achieve this, we develop a method to measure tunneling to the first subband energy level.

In order to demonstrate FIQC while avoiding the complicated TFET fabrication and analysis, we use BTBT MOS-CAP[9,10] which is the key part of the line-TFET (Fig. 1(a)). In these highly doped MOS-CAPs, BTBT occurs when band bending is strong, and empty states in the conduction band energetically overlap with occupied states in the valence band or vice-versa (Fig. 1(c)). The generation/recombination of minority carriers by BTBT is measured in AC mode as charging of the inversion capacitance $C_{inv}$ by the conductance $G_{BTBT}$

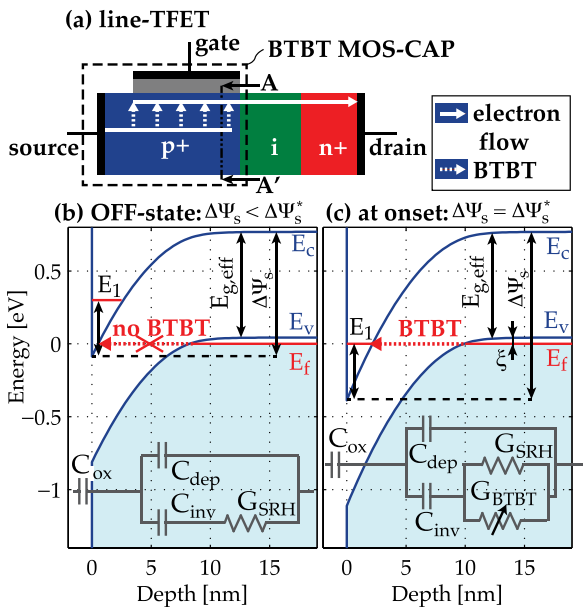


FIG. 1. (a) The line-TFET and BTBT MOS-CAP, of which the band diagrams along the cut line A-A' are shown (b) in off-state and (c) at BTBT onset. $E_c$ and $E_v$ are the conduction and valence band edges, $E_{g,eff} = E_c - E_v$ is the effective bandgap of the semiconductor, $E_1$ is the first subband energy, $E_f$ is the Fermi energy, and its degeneracy is $\xi = E_{v,bulk} - E_f$. The shaded areas depict occupied states. $\Delta\Psi_s$ is the semiconductor band bending and $\Delta\Psi_s^*$ is the same at BTBT onset. The insets show the equivalent circuit of the BTBT MOS-CAP.

a)Electronic mail: quentin.smets@imec.be

 

TABLE I. The samples are listed with their p-type dopant concentration ($N_A$) from Hall measurements, the thickness of $Al_2O_3$, and the electrically extracted value of $C_{ox}$.

| Samples | 1a | 1b | 2a | 2b | 3a | 3b | 4a | 4b |
|---|---|---|---|---|---|---|---|---|
| $N_A$ ($cm^{-3}$) | $1.3\times10^{19}$ | | $7.5\times10^{18}$ | | $4.4\times10^{18}$ | | $8.4\times10^{17}$ | |
| $t_{AlO}$ (nm) | 2 | 8 | 2 | 8 | 2 | 8 | 2 | 8 |
| $C_{ox}$ ($\mu F/cm^2$) | 2.0 | 0.76 | 2.2 | 0.75 | 2.0 | 0.74 | 2.2 | 0.75 |

(circuit in Fig. 1(c)). This is done at cryogenic temperature to suppress the capacitive response of oxide traps and the inversion build-up by thermal generation of minority carriers (conductance $G_{SRH}$). The electrostatics and charge distribution of BTBT MOS-CAP and line-TFET are identical in depletion and at onset (Figs. 1(b) and 1(c)). Therefore, we can verify the delayed onset of the line-TFET by measuring the inversion onset of a BTBT MOS-CAP at cryogenic temperature.

The MOS-CAP fabrication flow is as follows. 600 nm p-type doped $In_{0.53}Ga_{0.47}As$ (InGaAs) layers are epitaxially grown by MBE on 2-in. InP (001) substrates (also p-type doped $5\times10^{17}\,cm^{-3}$) from AXT Inc.[11] We use four different doping concentrations (Table I) to verify whether additional FIQC occurs with higher doping and at a correspondingly stronger electric field. After the growth, the native oxide is stripped with diluted HCl, and the surface is passivated with diluted ammonium sulfide. The samples are then immediately transferred to an Atomic Layer Deposition (ALD) chamber for the deposition of $Al_2O_3$ (either 2 or 8 nm) and $HfO_2$ (2 nm). The different oxide stacks allow us to verify whether traps in the oxide and at the oxide/InGaAs interface have a parasitic contribution to the C-V measurement. A TiN gate is deposited and patterned using dry etching. Finally, the backside of the substrates is contacted using AuZn/Au and the samples are annealed in forming gas.

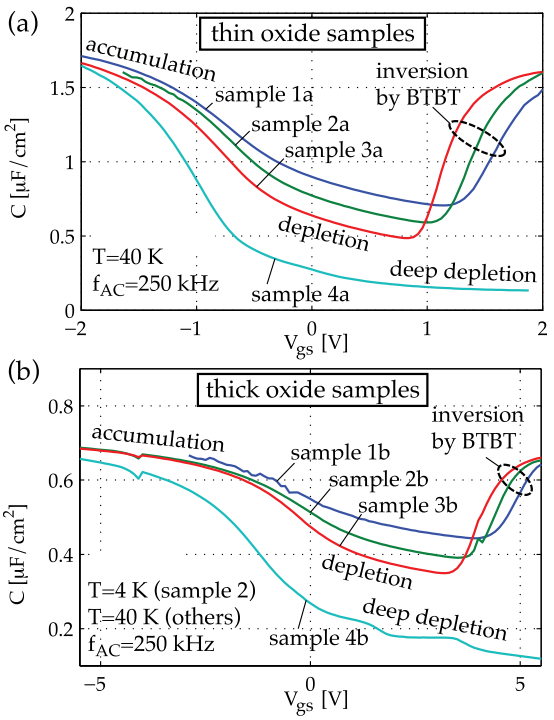


FIG. 2. C-V measurements of samples with (a) thin and (b) thick oxides show inversion by BTBT when the doping concentration is high. The curves are not shown when gate leakage is high. The fluctuations in capacitance at gate-source voltage $V_{gs} = -4$ V and 4 V are related to the measurement tool, and do not affect further interpretation of the results.

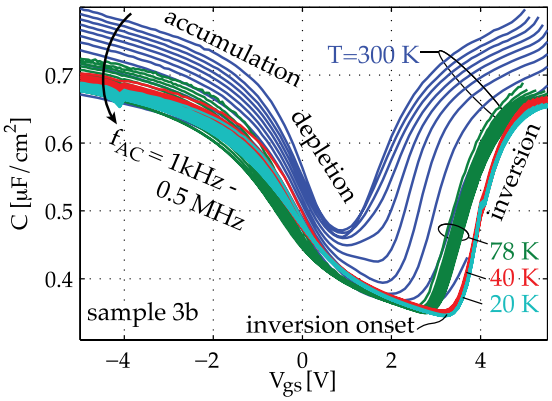


FIG. 3. Inversion generation is present at all measured temperatures, since BTBT is not a thermally activated process. Below T = 40 K, there is very little frequency dispersion near inversion onset, indicating a suppressed trap response.

InGaAs is chosen as semiconductor, because it still has a high tunneling probability when the depletion width, and hence the tunneling length, is as large as 10–20 nm. This large depletion width is necessary to accurately distinguish the depletion capacitance $C_{dep}$ from the oxide capacitance $C_{ox}$, which are both in series (Figs. 1(b) and 1(c)). InGaAs is doped p-type to reduce charging and discharging of parasitic interface traps when the MOS-CAP is biased near the BTBT onset condition. The Fermi level is then located in the conduction band, which is expected to have a lower amount of interface traps than the valence band.[11] Furthermore, a more accurate measurement of the quantization is possible, because it is stronger in the conduction band due to the lower density of states.

The C-V characteristics are determined with a Agilent 4284A precision LRC meter, and the curves are measured from inversion to accumulation. The equivalent parallel capacitance data of all samples at cryogenic temperature are shown in Fig. 2. Inversion generation by BTBT in samples 1a, 2a, 3a and 1b, 2b, 3b is evident from the following three arguments. First, inversion is present at all measured temperatures (Fig. 3), since BTBT is not a thermally activated process. Second, inversion is observed only with the highest doping concentrations (Fig. 2), where BTBT is efficient due

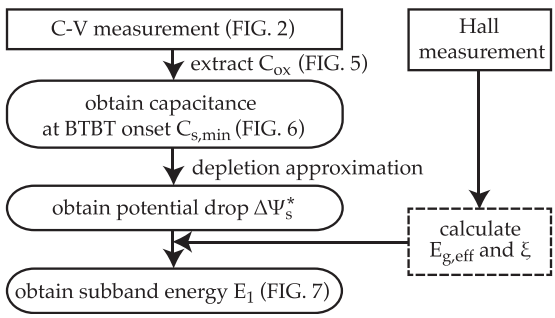


FIG. 4. The measurement of $E_1$ only requires C-V measurements and a Hall measurement. No complicated comparisons with simulations or input parameters other than $E_{g,eff}$, $\xi$ and the semiconductor dielectric constant $\epsilon_s$ are needed.

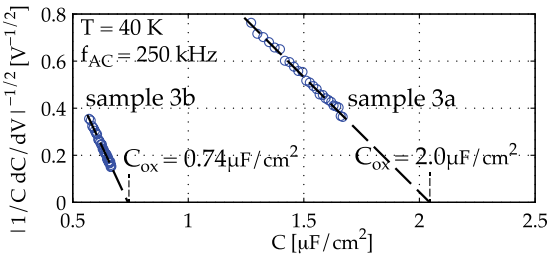


FIG. 5. The values of $C_{ox}$ listed in Table I are determined from extrapolation of the accumulation capacitance,[12] and at T = 40 K, a good linear fit is obtained for all samples and frequencies, as shown here for samples 3a and 3b and $f_{AC}$ = 250 kHz.

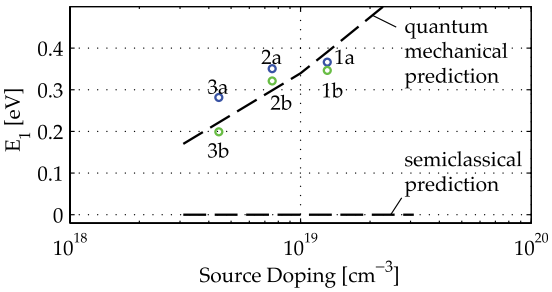


FIG. 7. $E_1$ obtained by experiments (symbols) agrees well with 15 band k·p quantum mechanical simulations, but not with the semiclassical prediction of any FIQC.

to the high electric field. For those samples, inversion is present at all AC frequencies $f_{AC}$ = 1 kHz–0.5 MHz without frequency dispersion (Fig. 3), since BTBT is very efficient at high electric fields. Finally, the inversion generation is not a perimeter effect, since the inversion capacitance scales with the MOS-CAP area (data not shown).

We extract the first subband energy level $E_1$ from the C-V results in Fig. 2 according to the procedure outlined in Fig. 4. The key objective is to determine $E_1$ from the potential drop over the semiconductor at the onset of inversion, $\Delta\Psi_s^*$ (Fig. 1(c)), which in turn is extracted from the value of the capacitance. Our procedure is different from previous work on Silicon BTBT MOS-CAP,[9] where $\Delta\Psi_s^*$ is extracted from the value of $V_{gs}$, because we observed that our measured C-V curves are stretched out in the $V_{gs}$ direction due to the charging of traps. The capacitance value at inversion onset is not impacted by traps, as verified by the absence of frequency dispersion at cryogenic temperature (Fig. 3). We therefore can extract $\Delta\Psi_s^*$ by first removing the $C_{ox}$ contribution (Fig. 5) from the measured complex impedance (capacitive part shown in Fig. 2), then select the imaginary part to obtain the semiconductor capacitance $C_s$ (Fig. 6). The onset of inversion is identified from the minimum of the latter, $C_{s,min}$, because at the corresponding value of $V_{gs}$ the extrapolated linear inversion capacitance reaches zero. This $V_{gs}$ is also the BTBT onset voltage of a line-TFET with identical semiconductor and gate stack.

In order to extract $\Delta\Psi_s^*$ from $C_{s,min}$ in a straightforward way, the depletion approximation is used: $\Delta\Psi_s^* = qN_A z_{d,max}^2/2\epsilon_s$

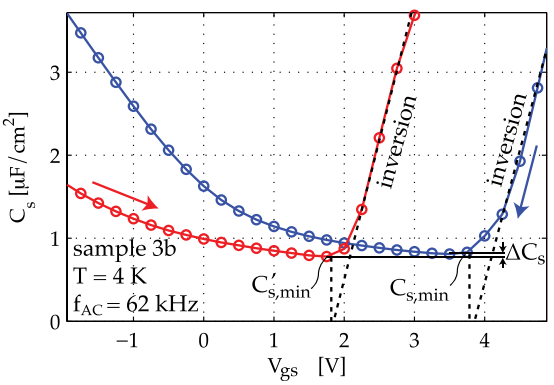


FIG. 6. $C_s$ at inversion onset $C_{s,min}$ is extracted by extrapolating the inversion capacitance to zero, coinciding with the point of minimum $C_s$. There is a small uncertainty $\Delta C_s$ on $C_{s,min}$ due to the measurement direction (full arrows), indicating the impact of interface charge on $E_1$.

with the maximum depletion width $z_{d,max} = \epsilon_s/C_{s,min}$. The validity of the depletion approximation for our range of doping concentrations and depletion widths was verified with Sentaurus Device,[13] and an error of less than 0.5% in $C_s$ is obtained at $\Delta\Psi_s^*$, which is satisfactory for our purpose.

$E_1$ is then calculated using $q\Delta\Psi_s^* = E_{g,eff} + \xi + E_1$ (Fig. 1(c)), where q is the electron charge and $\xi$ is the degeneracy or 0 if non-degenerate. $E_{g,eff}$ and $\xi$ are calculated based on the doping concentration and measurement temperature, and using Fermi-Dirac statistics and doping dependent band-gap narrowing.[14–16] The experimentally obtained values of $E_1$ show increasing FIQC for higher doping concentrations (circles in Fig. 7) due to the stronger electric field at onset. This FIQC observation is in agreement with previous C-V measurements on highly doped Silicon MOS-CAP,[17] where the inversion capacitance is generated thermally at T = 300 K instead of by BTBT. However, our FIQC observation is not in agreement with previous work on Silicon BTBT MOS-CAP,[9] where the very thick oxide (50–100 nm) most probably did not allow a sufficiently accurate measurement of $\Delta\Psi_s^*$. We compare our experimentally extracted onset of BTBT with predictions from a one-dimensional Schrödinger solver based on a 15-band k·p model and hard wall boundary conditions, and good agreement is obtained (Fig. 7). We conclude that FIQC indeed causes a delayed onset of BTBT.

There is an uncertainty on the obtained values of $E_1$ due to the sweep direction of $V_{gs}$ during the measurement (Fig. 6). When sweeping from accumulation to inversion, the curves are shifted to more negative $V_{gs}$, indicating an increase of positive trapped charge (or decrease of negative trapped charge), and $C_{s,min}$ is slightly lower, resulting in about 25% uncertainty on $E_1$ due to the difference with measurement direction. Simulations indicate that an increase of positive charge (or decrease of negative charge) at the interface, causing less steep band bending in the semiconductor, results in a higher first subband energy relative to the Fermi level. Therefore, a greater depletion width is required to reach BTBT onset. We also assess the sensitivity of $E_1$ to the different input parameters, and calculate that 10% variation on $N_A$ causes 30% variation on $E_1$. 10% variation on $C_{ox}$ causes 20%–40% variation on $E_1$, depending on the doping level. The high sensitivity on extracted $C_{ox}$ likely explains the systematically higher $E_1$ for samples 1a–3a compared with samples 1a–3b (Fig. 7). However, the total uncertainty on $E_1$ remains small compared with the absolute values

themselves, therefore, not affecting the conclusion that FIQC causes a delayed onset of BTBT.

BTBT MOS-CAPs show promise for trap characterization. First, hysteresis measurements show that $C_{s,min}$ is dependent on the sweep direction (Fig. 6) indicating that its value is a sensitive probe for the impact of interface traps on the semiconductor potential. Second, at low temperature, the value of $V_{gs}$ at BTBT onset provides a clear reference point for the $E_F$-$V_{gs}$ relationship, a challenge in lowly doped MOS-CAP due to a trap-induced $f_{AC}$-dependent threshold voltage shift.[18] When sweeping $V_{gs}$ between BTBT onset and flatband, the stretch-out of the C-V curves compared to the ideal C-V allows calculating the total charge trapped between these two $V_{gs}$. Third, it was shown that the Fermi level moves deep into the conduction band without Fermi level pinning, allowing the characterization of traps at this energy range. The response of the latter is shown by the frequency dispersion of the inversion capacitance at $T \geq 78$ K (Fig. 3). Finally, minority carrier generation by BTBT could allow the use of the full conductance method[18] to characterize interface traps without the need for MOSFET.

The delayed onset of BTBT due to FIQC, predicted by quantum mechanical simulations, was confirmed experimentally. Since FIQC occurs in nearly all TFETs, researchers should include it in all TFET simulations. The easy-to-fabricate BTBT MOS-CAP allows the measurement of the onset voltage of line-TFET, and are promising for the characterization of traps deep into the conduction band. The application of our method to heterostructure line-TFET with a staggered bandgap alignment[6] should be further explored.

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